PC Camera Controller

1. General Description

The SN9C102 is a single-chip backend processor to pair with the resolution of VGA or CIF CMOS image sensor. It reads the 9 or 8 bits input raw image data (RGB Bayer pattern) from an image capturing device and outputs through a USB port into the PC. This chip includes three individual digital color gains setting (named R, G, B gains), an image compression engine, an offset compensation, a hardware windowing with random image size selection, panning and scaling functions. Its multi-powerful functions and special architecture make this chip suitable for extra low cost USB PC camera application.

2. Features

- 9-Bit CMOS image raw data input
- Up to 30fps @ CIF, 12fps @VGA for PC mode video
- Provide individual R/G/B digital color gains control
- Provide snapshoot function
- Support pixel offset compensation
- Support *IC-media, ElecVision, TASC, Hynix, Pixart* ..etc
- Embedded two modes of AE calculation and report
- Provide hardware windowing, 1/2, 1/4 scaling function and panning function
- Support operation mode in image quality/frame rate selection
- USB 1.1 compliance and support suspend mode
- USB 4 endpoints: control, isochronous read, bulk read, and bulk write endpoints
- Support video data transfer either in USB isochronous or bulk modes
- Up to 9 alternated setting for USB isochronous transfer
- Up to 64 various P_ID in default mode and Random setting the P_ID, V_ID streaming
- 12MHz crystal and 3.3Volt only
- 48 pins LQFP package for normal function

3. PIN description

Number	NAME	I/O	Description
1	NC		
2	PID_SEL5	I	Product ID selection
3	PID_SEL4	I	Product ID selection
4	PID_SEL3	I	Product ID selection
5	PID_SEL2	I	Product ID selection
6	PID_SEL1	I	Product ID selection
7	PID_SEL0	I	Product ID selection
8	KEY	I	KEY input
9	RST	I	chip reset
10	NC		
11	NC		
12	AVDD	P	VDD for analog part
13	AVSS	P	GND for analog part
14	TAVSS	P	GND for USB part
15	DN	B	D- for USB
16	DP	B	D+ for USB
17	TAVDD	P	VDD for USB part
18	GPIO_0	B	General purpose I/O
19	GPIO_1	B	General purpose I/O
20	TEST	I	test mode
21	S_PWR_DN	O	Power down for sensor
22	LED	O	LED output
23	VDD	P	VDD for core
24	GND	P	GND for core
25	SDA	B	I2C data
26	SCL	O	I2C clock
27	S_PCK	B	Sensor pixel clock
28	VDD	P	VDD for core
29	GND	P	GND for core
30	SEN_CLK	O	Sensor clock
31	S_VSYNC	B	Sensor vsync
32	S_HSYNC	B	Sensor hsync
33	S_IMG0	B	Sensor image data
34	S_IMG1	B	Sensor image data
35	S_IMG2	B	Sensor image data
36	S_IMG3	B	Sensor image data

37	VDD	P	VDD for core
38	GND	P	GND for core
39	S_IMG4	B	Sensor image data
40	S_IMG5	B	Sensor image data
41	S_IMG6	B	Sensor image data
42	S_IMG7	B	Sensor image data
43	S_IMG8	B	Sensor image data
44	VDDAP	P	VDD for PLL
45	XIN	I	OSC input
46	XOUT	B	OSC output
47	VSSAP	P	GND for PLL
48	NC		

I : input pin , O : output pin , B : bi_direction pin , P : power pin .

4. Electrical Characteristics

4.1 DC Operating Condition

a. Absolute maximum ratings:

Symbol	Parameter	Rating	Units
Vcc	Power Supply	-0.3 to 3.6	V
Vin	Input Voltage	-0.3 to Vcc+0.3	V
Vout	Output Voltage	-0.3 to Vcc+0.3	V
Tstg	Storage Temperature	-55 to 150	°C

b. Recommended operating conditions:

Symbol	Parameter	Min	Typ	Max	Units
Vcc	Power Supply	3.0	3.3	3.6	V
Vin	Input voltage	0		Vcc	V
Topr	Operating Temperature	0		70	°C

c. DC electrical characteristics:

(Under Recommended Operating Conditions and Vcc=3.0 ~ 3.6V , Tj=0 to +115 °C)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Vil	Input low voltage	CMOS	-0.3		0.3Vcc	V
Vih	Input high voltage	CMOS	0.7Vcc		Vcc+0.3	V
Vil	Input low voltage	TTL	-0.3		0.8	V
Vih	Input high voltage	TTL	2.0		5.3	V
Iil	Input low current	no pull-up or pull-down	-1		1	uA
Iih	Input high current	no pull-up or pull-down	-1		1	uA
Ioz	Tri-state leakage current		-1		1	uA
Vil	Schmitt input low voltage	CMOS		1.20		V
Vih	Schmitt input high voltage	CMOS		2.10		V
Vol	Output Low voltage	Iol=4mA			0.4	V
Voh	Output high voltage	Ioh=4mA	2.4			V
Cin	Input capacitance			2.8		pF
Cout	Output capacitance		2.7		4.9	pF
Cbid	Bi-directional buffer Capacitance		2.7		4.9	pF

4.2 AC Operating Condition

Symbol	Description	Max operation Frequency	Notes
SEN_CLK	Sensor clock	48MHz	
XIN	Crystal input clock	12 MHz	
SCK	I2C clock frequency	400KHz	

5. USB interface

5.1 Endpoint description

Endpoint #	Function	Transfer Type	MaxPsz (byte)
0	STD Commands	Control	64
1	ISO Read	Isochronous	0, 128, 256, 384, 512, 680, 800, 900, 1023
2	Bulk Read	Bulk	64
3	Interrupt Read	Interrupt	1

5.2 Descriptor Table Data

Device	12 01 **10 01 00 00 00** 40 VL VH PL PH **01 01 00 01** 00 01
Configuration	09 02 17 01 01 01 00 **80 fa**
String	16 03 **55 00 53 00 42 00 20 00 63 00 61 00 6d 00 65 00 72 00 61 00**
Alternate Setting = 0	
Interface 0	09 04 00 00 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 00 00 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 1	
Interface 0	09 04 00 01 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 80 00 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 2	
Interface 0	09 04 00 02 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 00 01 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 3	
Interface 0	09 04 00 03 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 80 01 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 4	
Interface 0	09 04 00 04 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 00 02 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 5	
Interface 0	09 04 00 05 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 a8 02 01
Endpoint 2	07 05 82 02 40 00 00

Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 6	
Interface 0	09 04 00 06 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 20 03 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 7	
Interface 0	09 04 00 07 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 84 03 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**
Alternate Setting = 8	
Interface 0	09 04 00 08 03 **ff ff ff** 00
Endpoint 1	07 05 81 01 ff 03 01
Endpoint 2	07 05 82 02 40 00 00
Endpoint 3	07 05 83 03 01 00 **64**

6. Serial Control Interface

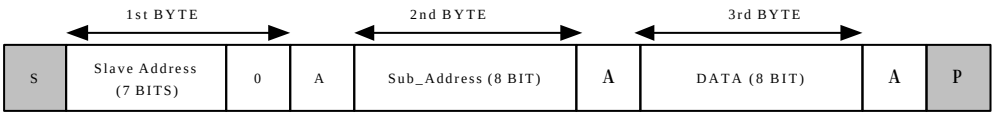
The SN9C102 supports I2C^{TM}-bus transfer protocol and is acting as a master device. It supports receiving and transmitting speed of 100kHz and 400kHz (Note: Downloading from EEPROM when power on requires speed of 400kHz.)

6.1 Serial Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) are needed to carry information between the devices connected to the serial bus. Normally both SDA and SCL lines are open-collector structures and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition: A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition.
- Valid data: The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. read/write control bit is the LSB of the first byte.
- Both the master and slave can transmit and receive data through the serial bus.
- Acknowledge: The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transfer by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

6.2 Data Transfer Format

- **Master device transmits data to slave device (write cycle)**
  - S : Start
  - A : Acknowledgement from slave device.
  - P : Stop
  - R/W : The LSB of 1st byte decides the current cycle is read or write. R/W=1 read ;R/W=0 write.
  - Slave Address : serial slave device address.
  - Sub Address : The slave device control register address.



Master transmits and Slave receives(write)

During write cycle, the master device(SONIX'S PC CAMERA CONTROLLER) generates start condition and then place the 1st byte data which contains slave address (7 bits) and the

Read/Write control bit onto SDA line. After slave device issues an acknowledgment, the master places the 2nd byte (sub-address data) data onto SDA line. And then followed the slave acknowledgment, the master places the 8 bits data on SDA line and transmits to slave device control register (address was assigned by 2nd byte). After slave issues an acknowledgment, the SN9C102 can generate a stop condition to end this write cycle. This chip only supports 8 bytes multiple write function. *That is, master can write only 8 contineous address data into slave device.*

▪ **Slave device transmits data to master device (read cycle)**

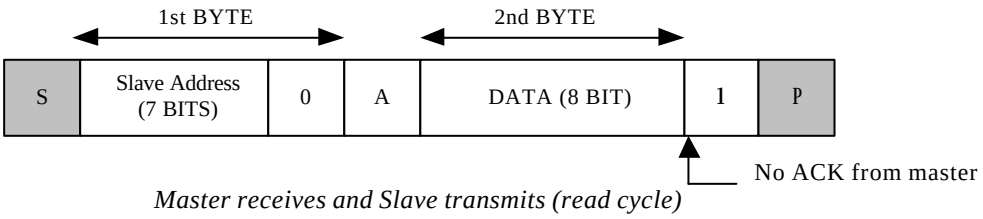
The read cycle of the SN9C102 has 2 phases, dummy write phase and read phase. *Note, this SN9C102 supports single read only.* That is, one dummy write phase plus one read phase can get only one byte data from slave device internal register.

a. The 1st phase (dummy write phase):

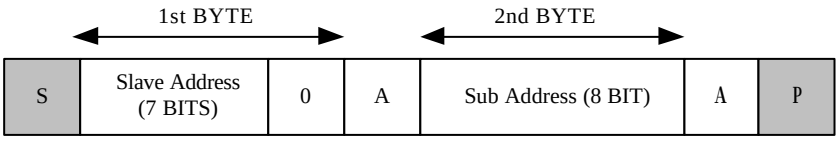
The dummy write phase is the same as the general serial write. The only difference is the write data is the address of the register. The Sub-Address is the register address inside the slave device

b. The 2nd phase (read phase) :

The *SN9C102* generates start condition and then place the 1st byte data, which contains slave address (7 bits) and a Read/Write control bit onto SDA line. After salve device issues an acknowledgment, the 8 bits data coming from slave device internal register will be placed onto the SDA line serially. The address of the 8 bit data was assigned by previous dummy write cycle. *Note, there is no acknowledgement issued by master device.*



Master receives and Slave transmits (read cycle)



Master transmits and Slave receives (Dummy write cycle)

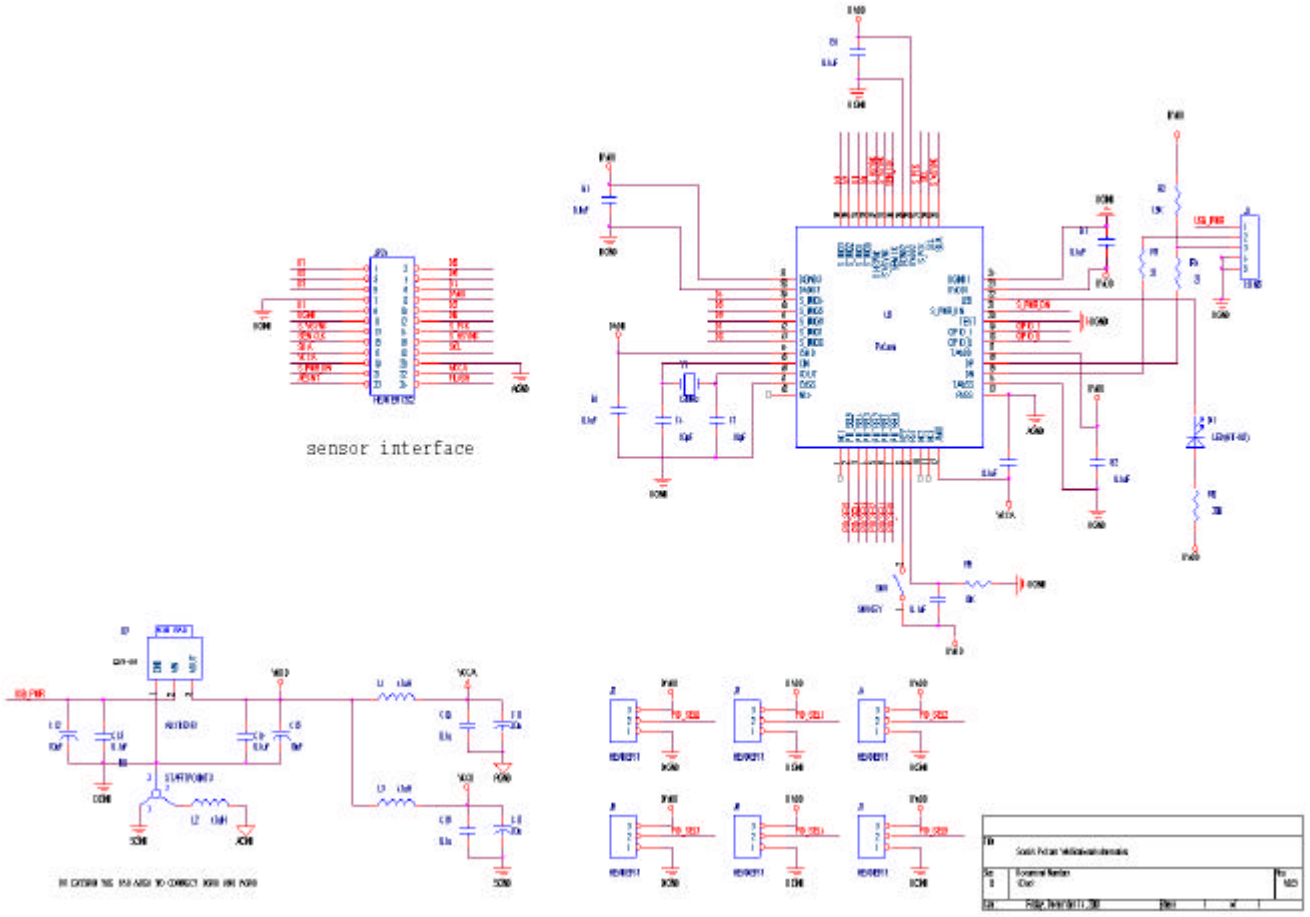
7. **Register description**

Address	Bit	R/W	Name	Description
0(00h)	7:0	R	ASIC_ID[7:0]	SONiX PC Cam chip ID (Return 10h)
1 (01h)	0	R/W	S_PWR_DN	1: Power down for sensor
	1	R/W	S_PDN_INV	1: Inverse pin S_PWR_DN
	2	R/W	V_TX_EN	1: Video transfer enable
	3	R/W	LED	Output to pin LED
	4	R	KEY	Read pin KEY
	5		Reserve	
	6	R/W	SYS_SEL_24M	1: System clock select 24MHz (Fsys_clk = 24 MHz) 0: System clock select 12MHz (Fsys _clk= 12 MHz)
	7	R/W	TEST_ASIC	1: Test mode enable for testing ASIC. Note: Don' t enable it
2	1:0	R/W	GPIO[1:0]	General purpose I/O
	7:2		Reserve	
3-7	7:0		Reserve	
8 (08h)	0	R/W	I2C_HIGH	1: I2C interface is high speed (400KHZ). 0: I2C interface is low speed (100KHZ).
	1	R/W	I2C_SEL_RD	1: Select I2C read mode. 0: Select I2C write mode.
	2	R	I2C_RDY	1: Ready for I2C read/write. 0: Busy for I2C read/write.
	3	R	I2C_ERR	I2C interface is error when read/write.
	6:4	R/W	I2C_BYTE_NUM[2:0]	I2C read/write byte number.
	7	R/W	I2C_DEV	1: Sensor interface is I2C. 0: Sensor interface is 3-wire interface.
9 (09h)	6:0	R/W	SLAVE_ID[6:0]	I2C slave ID
	7		Reserve	
10-14 (0a-0eh)	7:0	R/W	I2C_DATA[7:0]	Register read/write address and data port for I2C device Note: Write: You must write 5 bytes to it at one time. The first data is register address, the other data are data0, data1, data2 and data3. Read: You must read 5 bytes from it at one time. The sequence are data0, data1, data2, data3 and data4.
15 (0fh)	7:0	R/W	CONTROL/STATUS REGISTER	Control and status report byte
16 (10h)	3:0	R/W	R_GAIN[3:0]	Red channel gain control.→Gain = (1+R_GAIN/8) Note: It is sync with VSYNC
	7:4	R/W	B_GAIN[3:0]	Blue channel gain control.→Gain = (1+B_GAIN/8) Note: It is sync with VSYNC

17 (11h)	3:0	R/W	G_GAIN[3:0]	Green channel gain control.→Gain = (1+G_GAIN/8) Note: It is sync with VSYNC
	7:4		Reserve	
18 (12h)	7:0	R/W	H_START[7:0]	Start active pixel number after H-sync of sensor Note: The 1st line sequence of image data is BGBGBG The 2nd line sequence of image data is GRGRGR
19 (13h)	7:0	R/W	V_START[7:0]	Start active line number after V-sync of sensor
20 (14h)	7:0	R/W	OFFSET[7:0]	Offset adjustment for sensor image data.
21 (15h)	5:0	R/W	H_SIZE[5:0]	Horizontal pixel number for sensor.
	7:6		Reserve	
22 (16h)	4:0	R/W	V_SIZE[4:0]	Vertical pixel number for sensor.
	7:5		Reserve	
23 (17h)	0	R/W	LQ_SEL	1: Low quality for compression mode 0: High quality for compression mode
	1		Reserve	
	3:2	R/W	SEN_RATE	Sensor master clock frequency control 11: 48 MHz 10: 24 MHz 01: 12 MHz (default) 00: Fsys _clk /MCK_SIZE
	4	R/W	TEST_IMG	1: Image data is at test mode
	5	R/W	SEN_CLK_EN	1: Enable sensor clock. (Output to low)
	6	R/W	SEN_CLK_INV	1: Inverse SEN_CLK
	7		Reserve	
24 (18h)	0	R/W	PCK_RIS	1: Image data latch at rising edge of sensor PCK 0: Image data latch at falling edge of sensor PCK
	1	R/W	HSYNC_RIS	1: Change line at rising edge of HSYNC 0: Change line at falling edge of HSYNC
	2	R/W	VSYNC_RIS	1: Change frame at rising edge of VSYNC 0: Change frame at falling edge of VSYNC
	3	R/W	VSYNC_HIGH	1: VSYNC are high active. 0: VSYNC are low active.
	5:4	R/W	SCAL[1:0]	Resolution of sub-sampling before compression 00: 1/1 → (640*480), (352*288) 01: 1/2 → (320*240), (176*144) 1x: 1/4 → (160*120), (88*72)
	6	R/W	SEL_CURVE	0: Normal curve 1: Use companding curve
	7	R/W	CMP_MODE	Compression mode selection: 0: No compression for image data 1: Compression enable

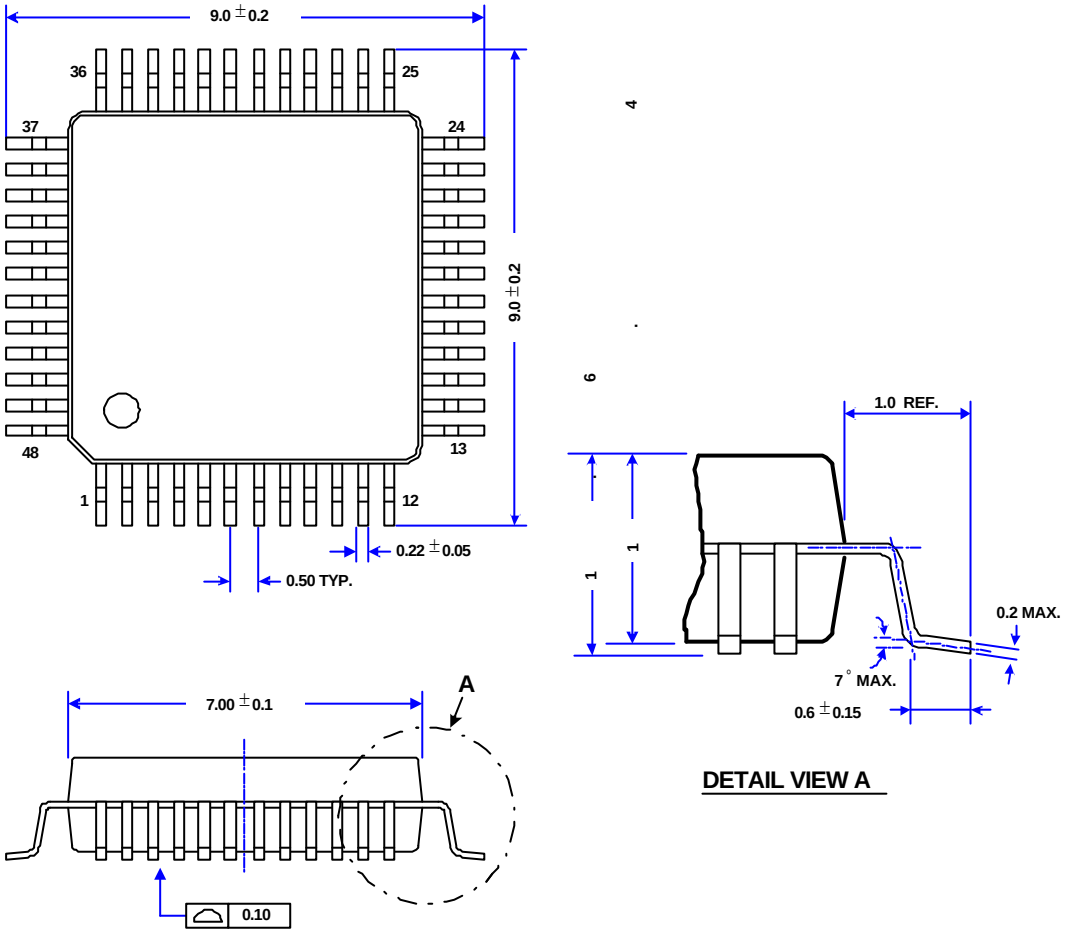
25 (19h)	0	R/W	SYNC_OUT	0: Sensor SYNC timing output disable. (Sensor is master mode) 1: Sensor SYNC timing output enable(Sensor is slave mode)
	1	R/W	PCK_OUT	0: Pixel clock input from pin “PCK”. 1: PCK_DATA output to PIN “PCK” and internal PCK is input from sensor master clock.
	2		Reserve	
	3	R/W	PCK_2X	1: Pixel clock period is 2 x master clock period. 0: Pixel clock period is 1 x master clock period. Note: It is valid when PCK_OUT=’ 1’
	7:4	R/W	MCK_SIZE[3:0]	Sensor master clock period size when SEN_RATE=0. (MCK_SIZE range is from 2 to 15) Note: Output frequency of master clock=(Fsys _clk /MCK_SIZE)
26 (1ah)	5:0	R/W	HO_SIZE[5:0]	Horizontal pixel number for sensor. (One unit is 32 pixels) Note: It is sync with VSYNC
	7:6		Reserve	
27 (1bh)	4:0	R/W	VO_SIZE[4:0]	Vertical pixel number for sensor. (One unit is 32 lines) Note: It is sync with VSYNC
	7:5		Reserve	
28 (1ch)	2:0	R/W	AE_STRX[2:0]	Start horizontal pixel for AE in active window. (One unit: 32 pixels)
	7:3		Reserve	
29 (1dh)	2:0	R/W	AE_STRY[2:0]	Start vertical line for AE in active window. (One unit: 32 pixels)
	7:3		Reserve	
30 (1eh)	4:0	R/W	AE_ENDX[4:0]	End horizontal pixel for AE in active window. (One unit: 32 pixels)
	7:5		Reserve	
31 (1fh)	3:0	R/W	AE_ENDY[3:0]	End vertical line for AE in active window. (One unit: 32 pixels)
	7:4		Reserve	

8. Application Circuit



9. Package Dimension

- **48pin LQFP**



(All dimensions are in Millimeters)